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in All Fields

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AND in All Fields

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```
(((instruction <and> translat* <and>
execut* <and> operating system <and>
simulat* <and> (interrupt <or> execption
<or> trap))<in>pdfdata)) <and> (pyr >=
1951 <and> pyr <= 2001)
```

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M Rosenblum, SA Herrod, E Witchel, A Gupta - Parallel & Distributed Technology: Systems & Applications, ..., 1995 - ieeexplore.ieee.org
... Although the direct-**execution** mode is fast, it provides ... uses on-the-fly object code **translation** to dynamically ... time and a breakdown of **instructions** executed. ...
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Talisman: fast and accurate multicomputer simulation - group of 10 »
RC Bedichek - Proceedings of the 1995 ACM SIGMETRICS joint international ..., 1995 - portal.acm.org
... Most direct **execution** simulators inspect and **translate** all m-**instructions** before **simulation** begins, ie, statically. ...
Cited by 66 - Web Search - BL Direct

Embra: fast and flexible machine simulation - group of 5 »
E Witchel, M Rosenblum - Proceedings of the 1996 ACM SIGMETRICS international ..., 1996 - portal.acm.org
... addressspaces.In addition to MMU **translation**, features of ... stop the current flow of **execution**, and invoke ... Embra needs to support **instructions** for manipulating ...
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M ROSENBLUM, E BUGNION, S DEVINE, SA HERROD - ACM Transactions on Modeling and Computer Simulation, 1997 - portal.acm.org
... of the actual interleaving of the **instructions** executed ... Direct **execution** was frequently used to position the workloads ... in favor of the binary **translation** approach ...
Cited by 210 - Web Search - BL Direct

EEL: machine-independent executable editing - group of 8 »
JR Larus, E Schnarr - Proceedings of the ACM SIGPLAN 1995 conference on ..., 1995 - portal.acm.org
... a solution to the **instruction**-set compatibility ... **translation** provides machines with the operations necessary ... edit executable to record **execution** frequencies or ...
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Superscalar **instruction execution** in the 21164 Alpha microprocessor - group of 3 »
JH Edmondson, P Rubinfeld, R Preston, V ... - Micro, IEEE, 1995 - ieeexplore.ieee.org
... in the memory unit and a 48 entry **instruction translation** buffer in the **instruction** unit. ... The integer and floating-point **execution** units are 6's- hits wide ...
Cited by 79 - Web Search - BL Direct

[BOOK] The Nachos Instructional **Operating System** - group of 20 »
WA Christopher, SJ Procter, TE Anderson - 1993 - eecs.berkeley.edu
... **system** kernel, and the hardware **simulator** run together in a ... sor workstation, including CPU **instruction execution**, address **translation**, interrupts, and ...
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Some efficient architecture simulation techniques - group of 11 »
R Bedichek - Winter 1990 Usenix Conference, 1990 - xsim.com
... **Execution** of delayed branches cause the decoded ip to be ... from the presence of a stale **translation** in the ... limit on the number of decoded **instruction** pages that ...
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PS Magnusson, F Dahlgren, H Grahn, M Karlsson, F ... - Proceedings of the 1998 USENIX Annual Technical Conference, 1998 - usenix.org
... benefit of running within a **simulator** is that ... read cache misses (data) (d) **translation** look-aside ... the **instruction** (g) count of **instruction execution** (h) flag ...

Published before January 2002
Terms used
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1 Performance of the VAX-11/780 translation buffer: simulation and measurement

Douglas W. Clark, Joel S. Emer
February 1985 **ACM Transactions on Computer Systems (TOCS)**, Volume 3 Issue 1
Publisher: ACM Press

Full text available: pdf(2.36 MB) Additional Information: full citation, abstract, references, citings, index terms

A virtual-address translation buffer (TB) is a hardware cache of recently used virtual-to-physical address mappings. The authors present the results of a set of measurements and simulations of translation buffer performance in the VAX-11/780. Two different hardware monitors were attached to VAX-11/780 computers, and translation buffer behavior was measured. Measurements were made under normal time-sharing use and while running reproducible synthetic time-sharing work loads. Reported measure ...

2 Efficient instruction cache simulation and execution profiling with a threaded-code interpreter

Peter S. Magnusson
December 1997 **Proceedings of the 29th conference on Winter simulation**
Publisher: ACM Press
Full text available: pdf(912.22 KB) Additional Information: full citation, references, index terms

3 Embra: fast and flexible machine simulation

Emmett Witchel, Mendel Rosenblum
May 1996 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1996 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '96**, Volume 24 Issue 1
Publisher: ACM Press

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This paper describes Embra, a simulator for the processors, caches, and memory systems of uniprocessors and cache-coherent multiprocessors. When running as part of the SimOS simulation environment, Embra models the processors of a MIPS R3000/R4000 machine faithfully enough to run a commercial operating system and arbitrary user applications. To achieve high simulation speed, Embra uses dynamic binary translation to generate code sequences which simulate the workload. It is the first machine simu ...

4 Shade: a fast instruction-set simulator for execution profiling

Bob Cmelik, David Keppel
May 1994 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the**